Avoiding Excessive Cross-terminal Voltages of Low Voltage Transistors Due to Undesirable Supply-Sequencing in Environments With Higher Supply Voltages

DESCRIPTION

(Para 1) Background of the Invention

(Para 2) Field of the Invention

(Para 3) The present invention relates to integrated circuits operating with multiple supply voltages of different magnitudes, and more specifically to a method and apparatus for avoiding excessive cross_terminal voltages of low voltage transistors due to undesirable supply_sequencing in environments with higher supply voltages.

(Para 4) Related Art

(Para 5) Integrated circuits are some times implemented with low voltage transistors in high voltage environments. A low voltage transistor is characterized by a correspondingly having a correspondingly low value for the maximum permissible cross terminal voltage. Exposure of the low voltage transistor to higher cross terminal voltage (than permissible cross terminal voltage) may reduce the lifetime of the low voltage transistor, as is well known in the relevant arts.

(Para 6) A high voltage environment is characterized by a high supply voltage (which is used to operate the various low voltage transistors). The word high implies that the supply voltage is more than the maximum permissible cross terminal voltage of the transistors. Using a high supply voltage generally provides a correspondingly high signal to noise ratio (SNR), typically leading to less susceptibility to noise in processing input signals.

(Para 7) Integrated circuits are often designed to operate with multiple supply voltages, with one or more of them constituting higher

supply voltages. Such multiple supply voltages with different magnitudes enable some portion of integrated circuits to operate from one magnitude of supply voltages, and other portions to operate from another magnitude of supply voltages.

(Para 8) Such designs may be chosen, for example, since low voltage transistors operate with higher throughput performance and low power consumption, and higher supply voltages may be used either to conform with interface specifications of external devices or for higher SNR, as noted above.

(Para 9) One problem with the use multiple supply voltages is that some supply voltages may be operational while others are not (operational), since some of such situations lead to applications of cross terminal voltages exceeding the maximum permissible values (noted above) when low voltage transistors are being operated with high supply voltages. Such excessive cross terminal voltages may be applied, for example, because portions of the integrated circuit which avoid such application, may be non-operational in the corresponding situation(s).

(Para 10) Such situations are of particularly likely to occur during the power-up or power-down of the devices using the integrated circuit since different supply voltages could "come up" (during power-up, or "come down" during power down) at different time instances, albeit within a short duration. The sequence in which the power supplies come up (or come down) is referred to as supply sequencing.

(Para 11) From the above, it may be appreciated that an undesirable supply sequencing may lead to excessive cross terminal voltages being applied across low voltage transistors. What is therefore needed is a method and apparatus to avoid excessive cross_terminal voltages of low voltage transistors due to undesirable supply_sequencing in environments with higher supply voltages.

(Para 12) Brief Description of the Drawings

(Para 13) The present invention will be described with reference to the following accompanying drawings.

(Para 14) Figure (Fig.) 1 is a block diagram illustrating the details of an example device in which various aspects of the present invention are implemented.

(Para 15) Figure 2 is a block diagram illustrating the details of a line driver in which various aspects of the present invention can be implemented.

(Para 16) Figure 3 is a circuit diagram of the details of a portion of the line driver illustrating the manner in which low voltage transistors can be exposed to excessive cross terminal voltages in an example scenario.

(Para 17) Figure 4 is a block diagram illustrating the manner in which exposure of low voltage transistors to excessive cross terminal voltages can be avoided according to an aspect of the present invention.

(Para 18) Figure 5 is a block diagram is a block diagram illustrating the implementation principle of various blocks of Figure 4 in one embodiment.

(Para 19) Figure 6 is a circuit diagram illustrating the implementation details of various blocks of Figure 4 in one embodiment.

(Para 20) Figure 7 is a timing diagram illustrating the operation of a buffer in one embodiment.

(Para 21) Detailed Description of the Preferred Embodiments

(Para 22) 1. Overview

(Para 23) An aspect of the present invention ensures that sufficient bias current is provided to a portion of a circuit ("circuit portion") containing low voltage transistors operating with a high supply voltage (having a magnitude greater than the maximum permissible cross terminal voltage of transistors contained in the circuit portion) irrespective of supply sequencing. Due to such a bias current, exposure of the transistors to excessive cross terminal voltages is avoided.

(Para 24) Such a sufficient bias current may be ensured by generating a primary bias current independent of PVT from a low supply voltage for high reliability, and a backup bias current from a high supply voltage, and providing the backup bias current as the bias current if the primary bias current is not present. The primary bias current may be provided as the bias current when the low supply voltage is available. Thus, the backup bias current is provided as bias current in case of undesirable supply sequencing.

(Para 25) Several aspects of the invention are described below with reference to examples for illustration. It should be understood that numerous specific details, relationships, and methods are set forth to provide a full understanding of the invention. One skilled in the relevant art, however, will readily recognize that the invention can be practiced without one or more of the specific details, or with other methods, etc. In other instances, well_known structures or operations are not shown in detail to avoid obscuring the invention.

(Para 26) 2. Example Device

(Para 27) Figure 1 is a block diagram of the details of an example device in which various aspects of the present invention can be implemented. Device 100 is shown containing processor 110, digital to analog converter (DAC) 120, low pass filter 130, and line driver 140. Each block is described below in further detail.

(Para 28) Processor 110 generates digital codes (on path 112), which need to be transmitted to external devices. DAC 120 converts the digital codes (received on path 112) into corresponding analog signals, and provides the analog signals on path 123. Low pass filter 130 performs filtering operation to remove unwanted frequency components from the analog signals generated by DAC 120, and the filtered signal is provided on path 134. Processor 110, DAC 120 and filter 130 may be implemented in a known way.

(Para 29) Line driver 140 receives the filtered signal on path 134, provides the filtered signal with a desired power/voltage level to drive transmission line 144. Line driver 140 further operates from low voltage supply 141 as well as high voltage supply 142. The high voltage supply has a magnitude greater than a maximum permissible voltage that can be applied across terminals of some transistors contained in line driver 140. Various aspects of the present invention protect such low voltage transistors from exposure against such excessive cross terminal voltages, when low voltage supply 141 is not present. The details of an embodiment of line driver 140 are described in further detail with reference to Figure 2.

(Para 30) 3. Line Driver

(Para 31) Figure 2 is a block diagram illustrating the details of line driver 140 in an embodiment of the present invention. Line driver 140 is shown containing low voltage portion block 210, bias current generator 220, and high voltage portion block 230. Each block is described below in further detail.

(Para 32) Low voltage portion block 210 operates from a low voltage supply (e.g., 3 V) received on path 141, and generates an amplified signal on path 213. In addition, a bias voltage signal is generated on path 212.

(Para 33) Bias current generator 220 generates a bias current on path 223 using both low voltage 141 and high voltage 142, and provides bias current to both low voltage portion block 210 and high voltage portion block 230. The details of implementation of an example embodiment of bias current generator 220 according to various aspects of the present invention, are described in sections below.

(Para 34) High voltage portion block 230 operates from a high voltage supply (e.g., 12 V) received on path 142, and generates an amplified signal which drives transmission line 144. High voltage portion block 230 is implemented using some low voltage transistors (e.g.,

transistors designed with 3V specification having a maximum permissible cross terminal voltage of 4V).

(Para 35) The bias current received on path 223 is used to protect low voltage transistors from receiving cross terminal voltages exceeding the maximum permissible voltage levels. The absence of bias current may expose the low voltage transistors to excessive cross terminal voltages, and damage the transistors as described below with reference to Figure 3.

(Para 36) 4. Damage to Transistors in the Absence of Bias Current

(Para 37) Figure 3 is a circuit diagram of a portion of high voltage portion block 230, illustrating the manner in which low voltage transistors can be damaged in the absence of bias current generated on path 223. The portion is shown containing NMOS transistors 315, 320, 360, 350, 380 and 370, and PMOS transistors 310, 330, 340, 390 and 395. It should be appreciated that the other portions of high voltage portion block 230 are not shown to avoid obscuring various aspects of the present invention.

(Para 38) Transistors 320 and 380, implemented as high voltage transistors, operate to protect transistors 350, 360 and 370 when bias current is present. The combination of transistors 315 and 350 operates as a current mirror. In the absence of low bias voltage 141, transistor 350 turns off, which will pull nodes 311 and 312 to high voltage supply 142. However, depending on the bias at the gate of 370 the potential at path 389 can go to ground which causes excess cross terminal voltage and may damage the transistor 390.

(Para 39)

(Para 40) Several other transistors also may be similarly damaged due to similar reasons. Accordingly, it is generally desirable that bias current be always provided when device 100 is operational (or powered on).

(Para 41) One possible reasons for the absence of such bias current on path 223 is that low voltage supply 141 is not present when high voltage supply 142 is present, for example, because of low voltage supply 141 'comes up' after high voltage supply 142 during initialization of device 100. The manner in which the presence of bias current can be ensured according to various aspects of the present invention is described below in further detail.

(Para 42) 5. Ensuring the Presence of Bias Current

(Para 43) Figure 4 is a block diagram illustrating the manner in which presence of bias current can be ensured according to various aspects of the present invention. The block diagram is shown containing primary bias current block 410, backup bias current block 420, comparator 430, and multiplexor 440. Each block is described below in detail.

(Para 44) Primary current block 410 generates primary bias current (on path 411) using low voltage supply 141. In the absence of low voltage supply 141, primary bias current is also absent. As described below in further detail, the primary bias current is provided as bias current 223 in normal operating conditions when low voltage supply 141 is available.

(Para 45) Backup current block 420 generates backup bias current (on path 422) using high voltage supply 142. Backup current block 420 may be designed to provide the same order of current as primary bias current to avoid damage to the low voltage transistors (e.g., 390).

(Para 46) The implementation of backup current block 420 and primary current block 410 will be apparent to one skilled in the relevant arts by reading the disclosure provided herein. In an embodiment, primary current block 410 is implemented to be independent of variations in PTV (process, temperature and voltage), while backup current block is not designed to meet such a criteria.

(Para 47) Comparator 430 compares the primary bias current (411) with the backup bias current (422) and generates a comparison result on path 434. Thus, the comparison result would equal one logical value when the primary bias current is present, and another value otherwise.

(Para 48) Multiplexor 440 selects one of primary bias current (411) and backup bias current (422) according to the comparison result received on path 434. The selected signal is provided on path 223. Thus, the primary bias current is provided on path 223 in normal operating conditions, and the backup bias current is provided when the primary bias current is absent.

(Para 49) Thus, by ensuring that backup bias current is present at least when the primary bias current is absent, damage to various low voltage transistors (in high voltage portion block 230) may be avoided.

(Para 50) The combination of the components of Figure 4 can be implemented using various approaches. The principle behind an example approach is described first, followed by corresponding implementation details.

(Para 51) 6. Implementation Principle

(Para 52) Figure 5 is a block diagram illustrating the principle of implementing the combination of primary current block 410, backup current block 420 and comparator 430 of Figure 4. The block diagram is shown containing current sources 510 and 520, and buffer 530. Each block is described below in further detail.

(Para 53) Buffer 530 operates to provide sharper transitions on path 434 in response to transitions occurring at node 512. Buffer 530 may also isolate from node 512 any components further down on path 434. Buffer 530 may be implemented in a known way (e.g., as two inverters connected in series).

(Para 54) Current sources 510 and 520 respectively represent primary current block 410 and backup current block 420, and are shown driving node 512. The currents from the two current sources drive node 512, but the current with higher magnitude determines the voltage level at node 512.

(Para 55) In one embodiment, current source 510 is designed have a magnitude of 2.5 times that of current source 520, which ensures that node 512 is logic ' 1In normal operating conditions. As soon as current source 510 becomes lower than 520, the voltage at node 512 starts going down. Thus, the voltage level (and thus the logic value eventually generated by buffer 530) at node 512 is determined by the strength of current in two current sources.

(Para 56) As noted above, under normal conditions, the magnitude of current source 510 is higher than that of current 520, and hence the voltage level at node 512 represents ' 1' . As a result, the output of buffer 530 would indicate whether the primary bias current or backup bias current is to be provided as the bias current on path 223. The description is continued with respect to an example implementation using the principle described above.

(Para 57) 7. Implementation Detail

(Para 58) Figure 6 is a circuit diagram illustrating the implementation details of the combination of primary current block 410 and backup current block 420 in one embodiment. The circuit diagram is shown containing PMOS transistors 610 and 620, NMOS transistors 630 and 640, current source 510 and resistor 660. Each component is described below.

(Para 59) Current source 510 provides primary bias current on path 411. The combination of PMOS transistors 610 and 620 operate as a current mirror circuit, and thus path 622 contains the same amount of current as on path 411. Current source 520 of Figure 5 is implemented

using NMOS transistors 630 and 640, and resistor 660, as will be apparent from the description below.

(Para 60) Resistor 660 receives high voltage supply 142 and generates backup bias current on path 422. The resistance value of 660 is chosen to generate backup bias current of a desired magnitude. The combination of NMOS transistors 630 and 640 operate as a current mirror, due to which path 644 would contain same current as on path 422. Paths 644 and 622 are connected at node 512.

(Para 61) It should be appreciated that the voltage at node 512 changes gradually when the two current sources are operative. However, buffer 530 operates to provide sharp transitions, as described below with reference to Figure 7.

(Para 62) Figure 7 is a timing diagram, with line 710 depicting the voltage at node 512 and line 750 depicting the output of buffer 530 on path 434. The peak voltage level of the two signals (710 and 750) equals the low voltage level 141. As can be readily observed, the transitions on line 750 are sharp compared to the gradual change on line 710.

(Para 63) Even though the examples above are described with reference to ensuring the presence of bias current in the absence of low voltage supply, the presence of bias current may be ensured in the absence of high voltage supply as well, as may be desirable in specific situations. Such implementations are covered by various aspects of the present invention.

(Para 64) 9. Conclusion

(Para 65) While various embodiments of the present invention have been described above, it should be understood that they have been presented by way of example only, and not limitation. Thus, the breadth and scope of the present invention should not be limited by any of the

above described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.